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[TITLE OF THE INVENTION]

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

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[CLAIMS]

1. A resin-encapsulated semiconductor device using
a lead frame which is shaped in accordance with a two-step
etching process to a body wherein a thickness of inner
10 leads is less than that of the lead frame blank,
comprising:

inner leads having the thickness less than that of the
lead frame blank; and

terminal columns integrally connected to the inner
15 leads and having the same thickness with the lead frame
blank, the terminal columns possessing a column-shaped
configuration which is adapted to be electrically connected
to an external circuit, the terminal columns being disposed
outside of the inner leads in a manner such that they are
20 coupled to the inner leads in a direction orthogonal to the
thickness-wise direction thereof, the terminal columns
having terminal portions arranged on top ends thereof, the
terminal portions being made of solders, etc. and exposed
to the outside beyond a resin encapsulate, each inner lead
25 possessing a rectangular cross-section and having four

surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising:

inner leads having the thickness less than that of the lead frame blank; and

terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank, while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

3. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

4. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

5. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

6. The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively.

7. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[DESCRIPTION OF THE PRIOR ART]

FIG. 15(a) shows the configuration of a generally known resin-encapsulated semiconductor device (a plastic lead frame package). The shown resin-encapsulated semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1513 to be electrically connected to the associated circuits, inner leads 1512 formed integrally with the outer leads 1513, bonding wires 1530 for electrically connecting the tips of the inner leads 1512 to the bonding pad 1521 of the semiconductor chip 1520, and a resin 1540 encapsulating the semiconductor chip 1520 to protect the semiconductor chip 1520 from external stresses and contaminants. This resin-encapsulated semiconductor device, after mounting the semiconductor chip 1520 on the bonding pad 1521, is manufactured by encapsulating the semiconductor chip 1520 with the resin. In this resin-encapsulated semiconductor device, the number of the inner leads 1512 is equal to that of the bonding pads 1521 of the semiconductor chip 1520. And, FIG. 15(b) shows the configuration of a monolayer lead frame used as an assembly member of the resin-encapsulated semiconductor device shown in FIG. 15a. Such a lead frame includes the bonding pad 1511 for mounting the semiconductor chip, the inner leads 1512 to be electrically connected to the semiconductor chip, the outer lead 1513 which is integral with the inner leads 1512 and is to be electrically connected to the associated circuits. This also includes dam bars 1514 serving as a dam when encapsulating the semiconductor chip with the resin, and a frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal such as a cobalt, 42 alloy (a 42% Ni-Fe alloy), copper-based alloy by a pressing working process or an etching process. FIG. 15(b)(D) is a cross-sectional view taken along the line F1-F2 of FIG. 15(b)(1).

Recently, there has been growing demand for the miniaturization and reduction in thickness of resin-encapsulated semiconductor device employing lead frames like the lead frame (plastic lead frame package) and the increase of the number of terminals of resin-encapsulated semiconductor package as electronic apparatuses are miniaturized progressively and the degree of the integration of semiconductor device increase progressively. Thus, recent resin-encapsulated semiconductor package, particularly quad plate package (QFPs) and thin quad flat packages (TQFPs) have each a greatly increased number of pins.

Lead frames having inner leads arranged at small pitches among lead frames for semiconductor packages are fabricated by a photolithographic etching process, while lead frames having inner leads arranged at comparatively large pitches among lead frames for semiconductor packages are fabricated by press working. However, lead frames having a large number of fine inner leads to be used for forming semiconductor packages having a large number of

pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

5 The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, a photoresist, such as a water-soluble casein photoresist containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

10 Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant containing ferric chloride as a principal component is sprayed against the thin sheet 1410 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1420 so that inner leads of predetermined sizes and shapes are formed as shown in FIG. 14(d).

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Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100% of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80 μ m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm is used and inner leads are formed by etching so that the

fine tips thereof are arranged at a pitch of about 0.1 mm.

However, recent miniature resin-encapsulated semiconductor package requires inner leads arranged at pitches in the range of 0.13 to 0.15 mm, far smaller than 0.165 mm. When a lead frame is fabricated by processing a thin sheet of a reduced thickness, the strength of the outer leads of such a lead frame is not large enough to withstand external forces that may be applied thereto in the subsequent processes including an assembling process and a chip mounting process. Accordingly, there is a limit to the reduction of the thickness of the thin sheet to enable the fabrication of a minute lead frame having fine leads arranged at very small pitches by etching.

An etching method previously proposed to overcome such difficulties subjects a thin sheet to an etching process to form a lead frame after reducing the thickness of portions of the thin sheet corresponding to the inner leads of the lead frame by half-etching or pressing to form the fine inner leads by etching without reducing the strength of the outer leads. However, problems arise in accuracy in the subsequent processes when the lead frame is formed by etching after reducing the thickness of the portions corresponding to the inner leads by pressing; for example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

15 (SUBJECT MATTERS TO BE SOLVED BY THE INVENTION)

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting process. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals

and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

(MEANS FOR SOLVING THE SUBJECT MATTERS)

5 According to one aspect of the present invention, there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns electrically connected to the inner leads and having the same thickness as the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond the resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead possessing a rectangular cross-section and having four surfaces including a

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surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention, a semiconductor chip is received inward of the inner leads, and electrodes (pads) of the semiconductor chip are electrically connected to the inner leads through wires, respectively. According to another aspect of the present invention, the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad. According to another aspect of the present invention, the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape. According to still another aspect of the present invention, the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

20 [WORKING FUNCTIONS]

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the forming process of the outer leads as in the case of using

a mono-layered lead frame shown in FIG. 13(b) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and coplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding process can be enlarged.

[EMBODIMENTS]

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, a resin-encapsulated semiconductor device in accordance

with a first embodiment of the present invention described hereinafter with reference to FIGs. 1. FIG. 1(a) is a cross-sectional view of the encapsulated semiconductor device according to the embodiment of the present invention. FIG. 1(b) is a sectional view of an inner lead taken along the line of FIG. 1(a), and FIG. 1(c) is a cross-sectional view of a terminal column taken along the line B1-B2 of FIG. 1. Moreover, FIG. 2(a) is a perspective view of the encapsulated semiconductor device according to the embodiment of the present invention, FIG. 2(b) is a view of the resin-encapsulated semiconductor device of FIG. 2(a), and FIG. 2(c) is a bottom view of the encapsulated semiconductor device of FIG. 2(a). In FIGs. 1 and 2, a drawing reference numeral 100 represents a resin-encapsulated semiconductor device, 110 a semiconductor chip, 111 electrodes (pads), 120 wires, 130 a lead frame, 131 inner leads, 131Aa a first surface, 131Ab a second surface, 131Ac a third surface, 131Ad a fourth surface, 132 terminal columns, 133A terminal portions, 133B side surfaces, 133S a top surface, 135 a die pad, and 140 a resin encapsulate.

In the resin-encapsulated semiconductor device according to the first embodiment, as shown in FIG. 1, the semiconductor chip 110 is placed inward of the

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 135 at one surface thereof which is opposed to the other surface thereof where the electrodes pads 111 of the semiconductor chip 110 are arranged. Each electrode pad 111 is electrically connected to the second surface 131A of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133A located on the top surfaces 133S of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-iron alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 or other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 9A is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40 μ m whereas the portions of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire bonding thereon. Also, as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed.

In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the inner leads 131 is long or not. The inner leads having the contour, as shown in FIG. 9(a), in which the tips of the inner leads 131 are separated one from another, are prepared by the etching process, and the inner leads are resin-encapsulated after mounting the semiconductor chip thereon as will be described later. However, where the inner leads 131 are long in their length and have a tendency for the generation of twisting therein, it is impossible to fabricate the lead frame by etching to have the contour as shown in FIG. 9(a). Therefore, after etching the lead frame in a state where the tips of the inner leads are fixed to the connecting portion 131B as shown in FIG. 9(c)(1), the inner leads 131 are fixed with the reinforcing tape 160 as shown in FIG. 9(c)(D). Then, the connecting portions 131B which are not necessary in the fabrication of the resin-encapsulated semiconductor device are removed by a press as shown in FIG. 9(c)(^), and a semiconductor device is then mounted on the lead frame.

Hereinafter, a method for the fabrication of the resin-encapsulated semiconductor device will now be described with reference to FIG. 8. First, the lead frame 130A, as shown in FIG. 9(a), which is shaped by the etching process as will be described later, is prepared such that the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are
5 directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131Ab of the inner leads 131 are bonded with each other using wires 120
10 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press
15 to form terminal columns 133 and also the side surfaces 133B of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi-
20 spherical solder are arranged on the outer surface of each terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the
25 resultant structure in such a manner that the side surfaces

of the terminal columns 133 are covered thereby FIG. 6(f)). At this time, the protective frame 180 functions to reinforce the semiconductor device. In other words, the protective frame 180 serves to prevent moisture from
5 leaking into a gap between the resin encapsulate and the terminal columns due to the fact that the side surfaces of the terminal columns are exposed to the outside, whereby a crack is not formed in the semiconductor device and the breakage of the semiconductor device is avoided. However,
10 persons skilled in the art will readily appreciate that it is not necessarily required to provide the protective frame 180. Also, when such an encapsulating process by the resin is carried out using a desired mold, the encapsulating process is implemented in a state wherein the outer side
15 surfaces of the terminal columns of the lead frame are somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first embodiment will now be described in conjunction with the attached drawings. FIG. 11 is of cross-sectional views
20 respectively illustrating sequential steps of the etching process for the lead frame of the first embodiment. In particular, the cross-sectional views of FIG. 1 correspond to a cross section taken along the line D1-D2 of FIG. 9(a). In FIG. 11, the reference numeral 1110 denotes a lead frame
25 blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1160 second concave portions, 1170 flat surfaces, and 1180 an etch-resistant layer. First, a water-soluble casein resist using potassium dichromate as a sensitive agent is coated
5 over both surfaces of the lead frame blank 1110 made of a 42% nickel-iron alloy and having a thickness of about 0.15 mm. Using desired pattern plates, the resist films are patterned to form resist patterns 1120A and 1120B having first opening 1130 and second openings 1140, respectively
10 (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead frame blank 1110 to have a flat etched bottom surface to a thickness smaller than that of the lead frame blank 1110 in a subsequent process. The second openings 1140 are adapted
15 to form desired shapes of tips of inner leads. Although the first opening 1130 includes at least an area forming the tips of the inner leads 1110, a topology generated by partially thinned portion by etching in a subsequent process can cause hindrance in a taping process or a
20 clamping process for fixing the lead frame. Thus, an area to be etched needs to be large without being limited to fine portions of the tips of the inner leads. Thereafter, both surfaces of the lead frame blank 1110 formed with the resist patterns are etched using a 48 Be' ferric chloride
25 solution of a temperature of 57°C at a spray pressure of

2.5 kg/cm². The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth h corresponding to $1/3$ of the thickness of the lead frame blank 1110. FIG. 11(c).

5. Although both surfaces of the lead frame blank 1110 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the resist pattern 1120B is formed. Subsequently, the surface provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Inctec Inc.) by a die coater to form an etch-resistant layer 1180 so as to fill up the first recesses 1150 and to cover the resist pattern 1120A (FIG. 11(c)).

It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that the etch-resistant layer 1180 be coated over the entire

portion of the surface formed with the first recesses
and first opening 1130, as shown in FIG. 11(c), because
it is difficult to coat the etch-resistant layer 1180 on
the surface portion including the first recesses.
5 Although the etch-resistant layer 1180 wax employed in
this embodiment is an alkali-soluble wax, any suitable
wax resistant to the etching action of the etchant solution
remaining somewhat soft during etching may be used.
The method for forming the etch-resistant layer 1180 is not limited
10 to the above-mentioned wax, but may be a wax of a UV-se
type. Since each first recess 1150 etched by the pre-
etching process at the surface formed with the paste
is adapted to form a desired shape of the inner lead track,
filled up with the etch-resistant layer 1180, it is
15 further etched in the following secondary etching process.
The etch-resistant layer 1180 also enhances the mechanical
strength of the lead frame blank for the second etching
process, thereby enabling the second etching process to be
conducted while keeping a high accuracy. It is
20 possible to enable a second etchant solution to be sprayed
at an increased spraying pressure, for example, 2.5 kg
or above, in the secondary etching process. The increased
spraying pressure promotes the progress of etching in the
direction of the thickness of the lead frame blank in
25 the secondary etching process. Then, the lead frame blank

subjected to a secondary etching process. In this secondary etching process, the lead frame blank 1110 is etched at its surface formed with first recesses 1130 having a flat etched bottom surface, to completely
5 perforate the second recesses 1160, thereby forming the tips of inner leads 131A (FIG. 11d)).

The bottom surface 1170 of each recess formed by the primary etching process is flat. However, both side surfaces of each recess positioned at opposite sides of the
10 bottom surface 1170 have a concave shape depressed toward the inside of the inner lead. Then, the lead frame blank is cleaned. After completion of the cleaning process, the etch-resistant layer 1180, and resist films (resist patterns 1120A and 1120B) are sequentially removed. Thus,
15 a lead frame 130A having a structure of FIG. 9(a) is obtained in which tips of the inner leads 131A are arranged at a fine pitch. The removal of the etch-resistant layer 1180 and resist films (resist patterns 1120A and 1120B) is achieved using a sodium hydroxide solution serving to
20 dissolve them.

The processes for manufacturing the lead frame as shown in FIG. 11, is to form by means of etching the lead frame having the tips of the inner leads used in this embodiment of the present invention, which have a thickness
25 less than that of the lead frame. Especially, the first

surfaces 131Aa of the tips of the inner leads as shown in
FIG. 1, are flushed with one surfaces of remaining portions
of the inner leads having the same thickness with the lead
frame while being opposed to the second surfaces 131Ab, and
5 the third and fourth surfaces are formed to have a concave
shape which is depressed toward the inside of the inner
leads. Where a semiconductor chip is mounted on the second
surfaces 131Ab of the inner leads by means of bumps for an
electrical connection therebetween, as in a semiconductor
10 device according to a third embodiment as will be described
hereinafter, an increased tolerance for the connection by
bumps is obtained when the second surface 131Ab has a
concave shape depressed toward the inside of the inner
lead. To this end, an etching method shown in FIG. 12 is
15 adopted in this case. The etching method shown in FIG. 12
is the same as that of FIG. 11 in association with its
primary etching process. After completion of the primary
etching process, the etching method is conducted in a
manner different from that of the etching method of FIG. 11
20 in that the second etching process is conducted at the side
of the first recesses 1150 after filling up the second
recesses 1160 by the etch-resist layer 1180, thereby
completely perforating the second recesses 1160. At this
time, by implementing the primary etching process, etching
25 at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 131Ab, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGs. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGs. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness t of the inner lead tip which is finally obtained. For example, where the blank has a thickness t reduced to 50 μ m, the inner leads can have a fineness corresponding to a lead width $W1$ of 100 μ m and a tip pitch p of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness t of about 30 μ m and a lead

width W_1 of 70 μm , it is possible to form inner leads having a fineness corresponding to an inner lead pitch p of 0.12 mm. Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness t and the lead width W_1 . That is to say, an inner lead tip pitch p up to 0.08 mm, a blank thickness up to 25 μm , and a lead width W_1 up to 40 μm can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(1). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(1) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 (a polyimide tape is generally used, as shown in FIG. 9(b)(A)). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(D), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereon. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(1)(a). The tip 131A has an etched flat surface (second surface) 131Ab which is substantially flat and therefore has a width W1 slightly greater than the width W2 of an opposite surface. The widths W1 and W2 (about 1000 μ m) are more than the width W at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(D)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(D)(a), there has particularly excellent in wire-bonding property, because
5 the etched flat surface does not have roughness. FIG. 13(A) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip
10 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared
15 to that of the etched flat surface of this first embodiment. FIG. 13(B) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this
20 case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(B). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(B)(a) or FIG. 13(B)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing
25 reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will be described hereinafter. FIGs. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGs. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified

example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby
5 an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor
10 device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4
15 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device,
20 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a
25 reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 220, and the semiconductor chip 210 is electrically connected at its electrodes (pads) 211 to the second surfaces 231Ab of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 210 is fastened together with the inner leads 231 by the reinforcing fastener tape 270. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230 as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(1), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(2), which performs a reinforcing function is used.

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGS. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG.

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of the this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of this third embodiment, the semiconductor chip 310 is fastened to the second surfaces 331Ab of the inner leads 331 by the bumps 311 thereby to be electrically connected to the second surfaces 331Ab. The lead frame 330 has a contour as shown in FIGs. 10(a) and 10(b), which is formed by the etching process of FIG. 11. As shown in FIG. 13(1)(b), both widths W1A and W2A (about 100 μ m) at top and bottom ends of the inner leads 331 are larger than a width WA at a center portion in a thickness-wise direction. Due to the fact that the second surfaces 331Ab of the inner leads 331 is depressed toward the inside of the inner leads and the first surfaces 331Aa are flat, a desired fineness can be obtained. Also, when the second surfaces 331Ab of the inner leads 331 are electrically connected to the semiconductor chip via bumps, easy connection can be accomplished as shown in FIG. 13(D)(b). Further, in the case of this third embodiment, as in the case of the first and second embodiments, the electrical connection between the resin-encapsulated semiconductor device 300 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 300 via the terminal portions 333A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 333A located on the top surfaces of the terminal

columns 333, respectively.

In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

portions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

5 Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line 10 B7-B8 of FIG. 7(b). Because an outer appearance of the semiconductor device of the this fourth embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing 15 reference numeral 400 represents a semiconductor device, 410 a semiconductor chip, 411 pads, 430 a lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surface, 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating 20 adhesive. In the semiconductor device of this fourth embodiment, one surface of the semiconductor chip 410 on which the pads 411 are disposed is fastened to the second 25

surfaces 431Ab of the inner leads 431 by the insul-
adhesive 470, and the pads 411 and the first surfaces
of the inner leads 431 are electrically connected with
other by wires 420. The semiconductor device of
5 fourth embodiment uses the same lead frame which is use
the third embodiment, which has the contour as shown
FIG. 10(a) and 10(b). Also, in the case of this fourth
embodiment, as in the case of the first and second
embodiments, the electrical connection between the res-
10 encapsulated semiconductor device 400 of this embodiment
and an external circuit is achieved by mounting the res-
encapsulated semiconductor device 400 via the terminal
portions 433A each being made of a semi-spherical solder
on a printed circuit substrate, with the terminal portio-
15 433A located on the top surfaces of the terminal column
433, respectively.

FIG. 7(d) is a cross-sectional view illustrating
modified example of the semiconductor device in accordance
with the fourth embodiment of the present invention. In
20 the modified example of the semiconductor device as shown
in FIG. 7(d), the terminal portions each comprising the
semi-spherical solder are not provided, and the top
surfaces of the terminal columns are directly used as the
terminal portions. Because the protective frame is not
25 used and the side surfaces 433B of the terminal columns 433

are exposed to the outside, a checking operation by a test, etc. can be easily performed.

[EFFECTS OF THE INVENTION]

5 The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having outer leads as shown in FIG. 13(b). As a result of this, the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem associated with coplanarity. In addition to these advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay time.

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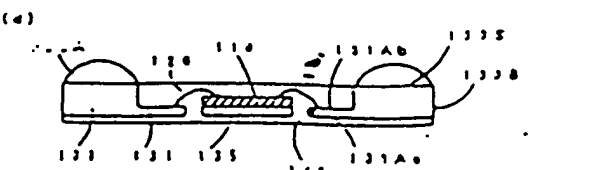
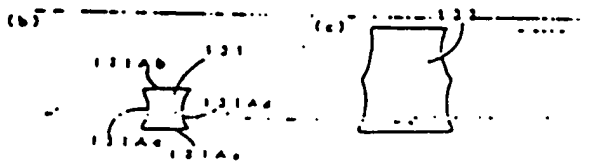
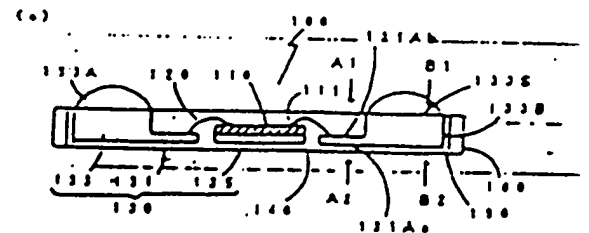
(54)【発明の名称】 紙層封止型平透体装置

(57)【要約】

(修正書)

【目的】 多層化に対応でき、且つ、フタリードの位置ずれや平透性の向上にも対応できる紙層封止型平透体装置を提供する。

【構成】 一体的に連結したリードフレーム部材と同じ部材の外側面と接続するための形状の端子部133とを有し、且つ、端子部はインナーリードの外側面においてインナーリードに対して厚み方向に突出して設けられており、端子部の先端面に半田等からなる端子膜を設け、端子部を封止層部から突出させ、端子部の外側面の側面を封止層部から突出させており、インナーリードは、断面形状が略方形で第1面131Aa、第2面Ab、第3面Ac、第4面Adの4面を有しており、かつ第1面はリードフレーム部材と同じ部材の端部の一方の面と同一平面上にあって第2面に向き合っており、第3面、第4面はインナーリードの内側に向かって凹んだ形状に形成されている。



【実施例 1】

2 段ニッチング加工によりインナーリードの厚さがリードフレーム素材の厚さよりも厚みになり、成形されたリードフレームを用いた半導体装置であって、前記リードフレームは、リードフレーム素材よりも厚みのインナーリードと、該インナーリードに一体的に連結したリードフレーム素材と同じ厚さの外側部材とを有する。該インナーリードは、断面形状が略方形であり、インナーリードの外表面においてインナーリードに対して厚み方向に直交して設けられており、該インナーリードの先端部を半導体素子からなる端子部と接続し、該端子部を封止用樹脂層から露出させ、該端子部の外表面の側面を封止用樹脂層から露出させており、インナーリードは、断面形状が略方形であり、かつ第 1 面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一平面上にあって第 2 面に向き合っており、第 3 面、第 4 面はインナーリードの内側に向かって凹んだ形状に形成されていることを特徴とする半導体装置。

【実施例 2】 2 段ニッチング加工によりインナーリードの厚さがリードフレーム素材の厚さよりも厚みになり、加工されたリードフレームを用いた半導体装置であって、前記リードフレームは、リードフレーム素材よりも厚みのインナーリードと、該インナーリードに一体的に連結したリードフレーム素材と同じ厚さの外側部材とを有する。該インナーリードは、断面形状が略方形であり、インナーリードの外表面においてインナーリードに対して厚み方向に直交して設けられており、該インナーリードの先端部を半導体素子からなる端子部と接続し、該端子部を封止用樹脂層から露出させて端子部とし、該端子部の外表面の側面を封止用樹脂層から露出させており、インナーリードは、断面形状が略方形であり、かつ第 1 面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一平面上にあって第 2 面に向き合っており、第 3 面、第 4 面はインナーリードの内側に向かって凹んだ形状に形成されていることを特徴とする半導体装置。

【実施例 3】 図 1 ないし 2 において、半導体素子はインナーリード間に設けられ、該半導体素子の電極部はワイヤにてインナーリードと電気的に接続されていることを特徴とする半導体装置。

【実施例 4】 図 3 において、リードフレームはダイパッドを有しており、半導体素子はダイパッド上に搭載され、固定されていることを特徴とする半導体装置。

【実施例 5】 図 3 において、リードフレームはダイパッドを持たないもので、半導体素子はインナーリードとともに樹脂固定用テープにより固定されていることを特徴とする半導体装置。

【実施例 6】 図 1 ないし 2 において、半導体素子は半導体素子の電極部をインナーリードの第 2 面

に絶縁性層を介して固定されており、該半導体素子の電極部はワイヤによりインナーリードの第 1 面と電気的に接続されていることを特徴とする半導体装置。

【実施例 7】 図 1 ないし 2 において、半導体素子はバンプによりインナーリードの第 2 面に固定されており、電気的にインナーリードと接続していることを特徴とする半導体装置。

【発明の効果】

(0001)

【従来の技術】 本発明は、半導体素子の多量に於いて対応で、且つ、アフターリードの位置ズレ（スキュー）やアフターリードの平坦性（コプラナリティー）の不良に起因する、リードフレームを用いた半導体装置に於ける。

(0002)

【従来の技術】 従来のように用いられている半導体装置（プラスチックリードフレームパッケージ）は、一般に図 1 (a) に示されるような構造であり、半導体素子 1510 を搭載するダイパッド 1511 の両側の区画との電気的接続を行うためのアフターリード 1513、アフターリード 1513 に一体となったインナーリード 1512、該インナーリード 1512 の先端部と半導体素子 1520 の電極パッド 1521 とを電気的に接続するためのワイヤ 1530、半導体素子 1520 を封止して外からの応力、熱から守る樹脂 1540 からなっており、半導体素子 1520 をリードフレームのダイパッド 1511 部上に搭載した場合には、樹脂 1540 により封止してパッケージとしたもので、半導体素子 1520 の電極パッド 1521 に対応する数のインナーリード 1512 を必要とするものである。そして、このような半導体装置の絶縁部材として用いられる（参照）リードフレームは、一般には図 1 (b) に示すような構造のもので、半導体素子 1520 を搭載するためのダイパッド 1511 と、ダイパッド 1511 の両側に設けられた半導体素子と接続するためのインナーリード 1512、該インナーリード 1512 に連結して外側部材との電気的接続を行うためのアフターリード 1513、半導体素子と接続する導体となる導体バー 1514、リードフレーム 1510 全体を支持するフレーム（基）部 1515 を備えており、通常、コパール、4 2 合金（42% ニッケル-合金）、銅合金のような導電性に優れた金属材料を用い、プレス加工もしくはエッチング法により形成されている。図 1 (b) (c) は、図 1 (b) (i) に示すリードフレームを基盤の F1-F2 における断面図である。

(0003) このようなリードフレームを用いた半導体装置の半導体素子（プラスチックリードフレームパッケージ）において、電極部との電気的接続の不良と半導体素子の劣化化に伴い、小型化かつ高集積度の

で、テーピングの工程や、リードフレームを固定するクランプ工程で、ベタ状に露出された部分的に腐食した部分との露出が異常になる場合があるので、エッチングを行うエリアはインナーリード先端の露出加工部分だけにせず大めにとる必要がある。次いで、温度 57°C 、比重 4.8 の塩化第二硫酸液を用いて、スプレーで 2.5 kg/cm^2 にて、レジストパターンが形成されたリードフレームを 1110 の位置をエッチングし、ベタ状（平箔状）に露出された第一の凹部 1150 の位置がリードフレーム露出部分の $2/3$ 程度に達した時点でエッチングを止めた。（図 11 (b)）

上記第 1 回目のエッチングにおいては、リードフレームを 1110 の位置から同時にエッチングを行ったが、必ずしも露出部分から同時にエッチングする必要はない。本実施例のように、第 1 回目のエッチングにおいてリードフレームを 1110 の位置から同時にエッチングする理由は、露出部分からエッチングすることにより、露出する第 2 回目のエッチング時間を短縮するため、レジストパターン 920 部からのみの露出エッチングの場合と比べ、第 1 回目エッチングと第 2 回目エッチングのトータル時間が短縮される。次いで、第一の凹部 1130 部の露出された第一の凹部 1150 部にエッチング液を 1180 としてのエッチング液のあるホットメルト型ワックス（ブレイクテニックス社のワックス、型番 MR-WB6）を、ダイコータを用いて、塗布し、ベタ状（平箔状）に露出された第一の凹部 1150 に埋め込んだ。レジストパターン 1120 A 上もエッチング液を 1180 に塗布された状態とした。（図 11 (c)）

エッチング液を 1180 を、レジストパターン 1120 A 上全面に塗布する必要はないが、第一の凹部 1150 を含む一帯にのみ塗布することは好ましい。図 11 (c) に示すように、第一の凹部 1150 とともに、第一の凹部 1130 部全面にエッチング液を 1180 を塗布した。本実施例で使用したエッチング液を 1180 は、アルカリ性塩基のワックスであるが、基本的にエッチング液に粘性があり、エッチング時に露出部分の腐食性のあるものが析出して、特に、上記ワックスに固定されて、U.V. 硬化型のものでもよい。このようにエッチング液を 1180 をインナーリード先端部の露出を形成するためのパターンが形成された露出部分の露出された第一の凹部 1150 に塗布することにより、露出部分のエッチング時に第一の凹部 1150 が露出部分で大きくならないようにしているとともに、露出部分のエッチング加工に對しての腐食性の低減を図っており、スプレー液を 2.5 kg/cm^2 以上とすることができ、これによりエッチングが露出部分に達しやすくなる。この後、第 2 回目のエッチングを行う。ベタ状（平箔状）に露出された第二の凹部 1160 部露出部分からリードフレームを 1110 をエッチングし、露出させ、

インナーリード先端部 131 A を形成した。（図 11 (c)）

第 1 回目のエッチング工程にて作成された、リードフレーム面に平坦なエッチング形成面に露出部分があるが、この露出部分 2 部はインナーリード側にへこんだ凹部である。次いで、洗浄、エッチング液を 980 の第 3 レジスト液（レジストパターン 1120 A、 1120 B）の液面を行い、インナーリード先端部 131 A が露出部分である図 9 (a) に示すリードフレーム 130 A を露出た。エッチング液を 1180 とレジスト液（レジストパターン 1120 A、 1120 B）の液面は露出部分トリウム水溶液により露出部分とした。

（図 11 (d)）上記、図 11 に示すリードフレームの露出部分には、本実施例に用いられる、インナーリード先端部を露出部分に形成したリードフレームをエッチング加工により露出する方式で、特に、図 11 に示す、インナーリード先端部の第 1 凹部 131 A を露出部分以外の露出部分と同一面に、第 2 凹部 131 B と対向させて形成し、且つ、第 3 凹部 131 C、第 4 凹部 131 D をインナーリードの内側に向かって凹んだ形状にするエッチング加工方式である。上述する実施例 3 の露出部分のようにパンプを露出部分にインナーリードの第 2 凹部 131 B に形成し、インナーリードと電気的に接続する場合に、

第 2 凹部 131 B をインナーリード側に凹んだ形状に形成した方がパンプ接続の時の接触面積が大きくなる。図 12 に示すエッチング加工方式が知られる。図 12 に示すエッチング加工方式は、第 1 回目のエッチング工程までは、図 11 に示す方式と同じであるが、エッチング液を 1180 を第二の凹部 1160 部に埋め込んだ後、第一の凹部 1150 部から第 2 凹部のエッチングを行い、露出部分で露出部分になっている。第 1 回目のエッチングにて、第二凹部 1140 からのエッチングを充分に行っており、図 12 に示すエッチング加工方式によって露出部分のリードフレームのインナーリード先端部の露出部分には、図 6 (b) に示すように、第 2 凹部 131 B がインナーリード側にへこんだ凹部になる。

（図 11 (e)）上記、図 11、図 12 に示すエッチング加工方式のように、エッチングを 2 段階にわたって行うエッチング加工方式を、一般には 2 段階エッチング加工方式という。上述加工に有利な加工方式である。本実施例に用いた図 9 (a) に示す、リードフレーム 130 A の露出部分においては、2 段階エッチング加工方式、パンプを露出部分に形成することにより部分的にリードフレームを露出したが、露出部分を露出部分とが露出部分に露出部分、リードフレームを露出部分とが露出部分に露出部分、露出部分加工が露出部分に露出部分、図 11、図 12 に示す、上述の方式においては、インナーリード先端部 131 A の露出部分加工は、第二の凹部 1160 の露出部分、露出部分に露出部分インナーリード先端部の露出部分に露出部分露出部分、例えば、露出部分 $50\text{ }\mu\text{m}$

同じとなるが、図に示した、面3や、20の位置関係
を、210は半導体基子、211は基板部（パッ
ド）、220はワイヤ、230はリードフレーム、23
1はゲージ・リーード、232は上面、233は下面、
234は第2面、231Aには第3面、231Bには第4面、
233には第1面、233Aには第5面、233Bには第
6面、233Cには上表面、240には片止溝部、270は
導物固定用テープある。また、図2の半導体装置におい
ては、リードフレーム230はダイパッドを持たないし
ので、半導体基子210はリターン・リーード231を中心とし
て導物固定用テープ270により固定されており、半導
体基子210は、半導体基子の外面部（パッド）211

例はワイヤ220により、インターリード231の第2面231A0と接続されている。本実施例2の場合も、実施例1の場合と同様に、半導体装置200と基板回路との電気的な接続は、端子E233の先端部に設けられた半導体装置の端子からなる端子部233Aを介してプリント基板面へ接続されることにより行われる。

(0020) また、本実施例2の半導体装置は、図10(a)、10(b)に示す、ダイパッドを用いた、ニッチングにより形成加工されたリードフレーム230Aを用いたもので、その製造方法には実施例1とはほぼ同じ工程であるが、異なる点は、実施例1の場合には半導体装置をインターリードに固定した状態でワイヤボンディングを行い、基板封止しているのに対し、本実施例2の場合には、半導体装置210をインターリード231とともに基板固定用テープ270上に固定した状態で、ワイヤボンディング工程を行い、基板封止している点である。尚、基板封止後のプレスによる半導体装置の端子部の形成は、実施例1と同様である。図10(a)に示すリードフレーム230Aを造るには、図9(a)に示すリードフレーム130Aを造る場合と同様にして、図9(b)に示す状態で「(イ)」に示すニッチング加工を施すものを用いる。図10(a)に示す形状にする。この時、図10(c)、(c)に示すように、導電性のため基板テープ260(ポリイミドテープ)を使用する。

(0021) 図5(a)～図5(c)に、実施例2の半導体装置の外形例半導体装置の断面図である。図5(a)に示す実施例2の半導体装置は、半導体装置の面が図5(a)で、基板面を有する面を下面にしている。およびワイヤボンディング面をリードフレームの第1面に設けて、その面が実施例2の半導体装置と見なす。図5(b)、図5(c)に示す実施例2の半導体装置は、それぞれ実施例2の半導体装置、図5(a)に示す実施例2の半導体装置に対して、半導体装置の端子からなる端子部を設け、端子部の面を基板面として用いているものである。図5(a)に示す、端子部233の側面233Bを露出している。テスト面での信号のチェックがし易い構造となっている。

(0022) 次に、実施例3の基板封止型半導体装置を説明する。図6(a)は実施例3の基板封止型半導体装置の断面図であり、図6(b)は図6(a)のA5-A6におけるインターリード部の断面図で、図6(c)は図6(a)の55-B6における端子部Eの断面図である。尚、実施例3の半導体装置の外形は実施例1とはほぼ同じとなる。図に示した、図6中、300は半導体装置、310は半導体装置、312はパンプ、330Cはリードフレーム、331はインターリード、331Aは第1面、331Abは第2面、331Acは第3面、331Adは第4面、331Aeは第5面、331Afは第6面、331Agは第7面、331Ahは第8面、331Aiは第9面、331Ajは第10面、331Akは第11面、331Alは第12面、331Amは第13面、331Anは第14面、331Aoは第15面、331Apは第16面、331Aqは第17面、331Arは第18面、331Asは第19面、331Atは第20面、331Auは第21面、331Avは第22面、331Awは第23面、331Axは第24面、331Ayは第25面、331Azは第26面、331Baは第27面、331Bbは第28面、331Bcは第29面、331Bdは第30面、331Beは第31面、331Bfは第32面、331Bgは第33面、331Bhは第34面、331Biは第35面、331Bjは第36面、331Bkは第37面、331Blは第38面、331Bmは第39面、331Bnは第40面、331Boは第41面、331Bpは第42面、331Bqは第43面、331Brは第44面、331Bsは第45面、331Btは第46面、331Buは第47面、331Bvは第48面、331Bwは第49面、331Bxは第50面、331Byは第51面、331Bzは第52面、331Caは第53面、331Cbは第54面、331Ccは第55面、331Cdは第56面、331Ceは第57面、331Cfは第58面、331Cgは第59面、331Chは第60面、331Ciは第61面、331Cjは第62面、331Ckは第63面、331Clは第64面、331Cmは第65面、331Cnは第66面、331Coは第67面、331Cpは第68面、331Cqは第69面、331Crは第70面、331Csは第71面、331Ctは第72面、331Cuは第73面、331Cvは第74面、331Cwは第75面、331Cxは第76面、331Cyは第77面、331Czは第78面、331Daは第79面、331Dbは第80面、331Dcは第81面、331Ddは第82面、331Deは第83面、331Dfは第84面、331Dgは第85面、331Dhは第86面、331Diは第87面、331Djは第88面、331Dkは第89面、331Dlは第90面、331Dmは第91面、331Dnは第92面、331Doは第93面、331Dpは第94面、331Dqは第95面、331Drは第96面、331Dsは第97面、331Dtは第98面、331Duは第99面、331Dvは第100面、331Dwは第101面、331Dxは第102面、331Dyは第103面、331Dzは第104面、331Eaは第105面、331Ebは第106面、331Ecは第107面、331Edは第108面、331Eeは第109面、331Efは第110面、331Egは第111面、331Ehは第112面、331Eiは第113面、331Ejは第114面、331Ekは第115面、331Elは第116面、331Emは第117面、331Enは第118面、331Eoは第119面、331Epは第120面、331Eqは第121面、331Erは第122面、331Esは第123面、331Etは第124面、331Euは第125面、331Evは第126面、331Ewは第127面、331Exは第128面、331Eyは第129面、331Ezは第130面、331Faは第131面、331Fbは第132面、331Fcは第133面、331Fdは第134面、331Feは第135面、331Ffは第136面、331Fgは第137面、331Fhは第138面、331Fiは第139面、331Fjは第140面、331Fkは第141面、331Flは第142面、331Fmは第143面、331Fnは第144面、331Foは第145面、331Fpは第146面、331Fqは第147面、331Frは第148面、331Fsは第149面、331Ftは第150面、331Fuは第151面、331Fvは第152面、331Fwは第153面、331Fxは第154面、331Fyは第155面、331Fzは第156面、331Gaは第157面、331Gbは第158面、331Gcは第159面、331Gdは第160面、331Geは第161面、331Gfは第162面、331Ggは第163面、331Ghは第164面、331Giは第165面、331Gjは第166面、331Gkは第167面、331Glは第168面、331Gmは第169面、331Gnは第170面、331Goは第171面、331Gpは第172面、331Gqは第173面、331Grは第174面、331Gsは第175面、331Gtは第176面、331Guは第177面、331Gvは第178面、331Gwは第179面、331Gxは第180面、331Gyは第181面、331Gzは第182面、331Haは第183面、331Hbは第184面、331Hcは第185面、331Hdは第186面、331Heは第187面、331Hfは第188面、331Hgは第189面、331Hhは第190面、331Hiは第191面、331Hjは第192面、331Hkは第193面、331Hlは第194面、331Hmは第195面、331Hnは第196面、331Hoは第197面、331Hpは第198面、331Hqは第199面、331Hrは第200面、331Hsは第201面、331Htは第202面、331Huは第203面、331Hvは第204面、331Hwは第205面、331Hxは第206面、331Hyは第207面、331Hzは第208面、331Iaは第209面、331Ibは第210面、331Icは第211面、331Idは第212面、331Ieは第213面、331Ifは第214面、331Igは第215面、331Ihは第216面、331Iiは第217面、331Ijは第218面、331Ikは第219面、331Ilは第220面、331Imは第221面、331Inは第222面、331Ioは第223面、331Ipは第224面、331Iqは第225面、331Irは第226面、331Isは第227面、331Itは第228面、331Iuは第229面、331Ivは第230面、331Iwは第231面、331Ixは第232面、331Iyは第233面、331Izは第234面、331Jaは第235面、331Jbは第236面、331Jcは第237面、331Jdは第238面、331Jeは第239面、331Jfは第240面、331Jgは第241面、331Jhは第242面、331Jiは第243面、331Jjは第244面、331Jkは第245面、331Jlは第246面、331Jmは第247面、331Jnは第248面、331Joは第249面、331Jpは第250面、331Jqは第251面、331Jrは第252面、331Jsは第253面、331Jtは第254面、331Juは第255面、331Jvは第256面、331Jwは第257面、331Jxは第258面、331Jyは第259面、331Jzは第260面、331Kaは第261面、331Kbは第262面、331Kcは第263面、331Kdは第264面、331Keは第265面、331Kfは第266面、331Kgは第267面、331Khは第268面、331Kiは第269面、331Kjは第270面、331Kkは第271面、331Klは第272面、331Kmは第273面、331Knは第274面、331Koは第275面、331Kpは第276面、331Kqは第277面、331Krは第278面、331Ksは第279面、331Ktは第280面、331Kuは第281面、331Kvは第282面、331Kwは第283面、331Kxは第284面、331Kyは第285面、331Kzは第286面、331Laは第287面、331Lbは第288面、331Lcは第289面、331Ldは第290面、331Leは第291面、331Lfは第292面、331Lgは第293面、331Lhは第294面、331Liは第295面、331Ljは第296面、331Lkは第297面、331Llは第298面、331Lmは第299面、331Lnは第300面、331Loは第301面、331Lpは第302面、331Lqは第303面、331Lrは第304面、331Lsは第305面、331Ltは第306面、331Luは第307面、331Lvは第308面、331Lwは第309面、331Lxは第310面、331Lyは第311面、331Lzは第312面、331Maは第313面、331Mbは第314面、331Mcは第315面、331Mdは第316面、331Meは第317面、331Mfは第318面、331Mgは第319面、331Mhは第320面、331Miは第321面、331Mjは第322面、331Mkは第323面、331Mlは第324面、331Mmは第325面、331Mnは第326面、331Moは第327面、331Mpは第328面、331Mqは第329面、331Mrは第330面、331Msは第331面、331Mtは第332面、331Muは第333面、331Mvは第334面、331Mwは第335面、331Mxは第336面、331Myは第337面、331Mzは第338面、331Naは第339面、331Nbは第340面、331Ncは第341面、331Ndは第342面、331Neは第343面、331Nfは第344面、331Ngは第345面、331Nhは第346面、331Niは第347面、331Njは第348面、331Nkは第349面、331Nlは第350面、331Nmは第351面、331Nnは第352面、331Noは第353面、331Npは第354面、331Nqは第355面、331Nrは第356面、331Nsは第357面、331Ntは第358面、331Nuは第359面、331Nvは第360面、331Nwは第361面、331Nxは第362面、331Nyは第363面、331Nzは第364面、331Oaは第365面、331Obは第366面、331Ocは第367面、331Odは第368面、331Oeは第369面、331Ofは第370面、331Ogは第371面、331Ohは第372面、331Oiは第373面、331Ojは第374面、331Okは第375面、331Olは第376面、331Omは第377面、331Onは第378面、331Ooは第379面、331Opは第380面、331Oqは第381面、331Orは第382面、331Osは第383面、331Otは第384面、331Ouは第385面、331Ovは第386面、331Owは第387面、331Oxは第388面、331Oyは第389面、331Ozは第390面、331Paは第391面、331Pbは第392面、331Pcは第393面、331Pdは第394面、331Peは第395面、331Pfは第396面、331Pgは第397面、331Phは第398面、331Piは第399面、331Pjは第400面、331Pkは第401面、331Plは第402面、331Pmは第403面、331Pnは第404面、331Poは第405面、331Ppは第406面、331Pqは第407面、331Prは第408面、331Psは第409面、331Ptは第410面、331Puは第411面、331Pvは第412面、331Pwは第413面、331Pxは第414面、331Pyは第415面、331Pzは第416面、331Qaは第417面、331Qbは第418面、331Qcは第419面、331Qdは第420面、331Qeは第421面、331Qfは第422面、331Qgは第423面、331Qhは第424面、331Qiは第425面、331Qjは第426面、331Qkは第427面、331Qlは第428面、331Qmは第429面、331Qnは第430面、331Qoは第431面、331Qpは第432面、331Qqは第433面、331Qrは第434面、331Qsは第435面、331Qtは第436面、331Quは第437面、331Qvは第438面、331Qwは第439面、331Qxは第440面、331Qyは第441面、331Qzは第442面、331Raは第443面、331Rbは第444面、331Rcは第445面、331Rdは第446面、331Reは第447面、331Rfは第448面、331Rgは第449面、331Rhは第450面、331Riは第451面、331Rjは第452面、331Rkは第453面、331Rlは第454面、331Rmは第455面、331Rnは第456面、331Roは第457面、331Rpは第458面、331Rqは第459面、331Rrは第460面、331Rsは第461面、331Rtは第462面、331Ruは第463面、331Rvは第464面、331Rwは第465面、331Rxは第466面、331Ryは第467面、331Rzは第468面、331Saは第469面、331Sbは第470面、331Scは第471面、331Sdは第472面、331Seは第473面、331Sfは第474面、331Sgは第475面、331Shは第476面、331Siは第477面、331Sjは第478面、331Skは第479面、331Slは第480面、331Smは第481面、331Snは第482面、331Soは第483面、331Spは第484面、331Sqは第485面、331Srは第486面、331Ssは第487面、331Stは第488面、331Suは第489面、331Svは第490面、331Swは第491面、331Sxは第492面、331Syは第493面、331Szは第494面、331Taは第495面、331Tbは第496面、331Tcは第497面、331Tdは第498面、331Teは第499面、331Tfは第500面、331Tgは第501面、331Thは第502面、331Tiは第503面、331Tjは第504面、331Tkは第505面、331Tlは第506面、331Tmは第507面、331Tnは第508面、331Toは第509面、331Tpは第510面、331Tqは第511面、331Trは第512面、331Tsは第513面、331Ttは第514面、331Tuは第515面、331Tvは第516面、331Twは第517面、331Txは第518面、331Tyは第519面、331Tzは第520面、331Uaは第521面、331Ubは第522面、331Ucは第523面、331Udは第524面、331Ueは第525面、331Ufは第526面、331Ugは第527面、331Uhは第528面、331Uiは第529面、331Ujは第530面、331Ukは第531面、331Ulは第532面、331Umは第533面、331Unは第534面、331Uoは第535面、331Upは第536面、331Uqは第537面、331Urは第538面、331Usは第539面、331Utは第540面、331Uvは第541面、331Uwは第542面、331Uxは第543面、331Uyは第544面、331Uzは第545面、331Vaは第546面、331Vbは第547面、331Vcは第548面、331Vdは第549面、331Veは第550面、331Vfは第551面、331Vgは第552面、331Vhは第553面、331Viは第554面、331Vjは第555面、331Vkは第556面、331Vlは第557面、331Vmは第558面、331Vnは第559面、331Voは第560面、331Vpは第561面、331Vqは第562面、331Vrは第563面、331Vsは第564面、331Vtは第565面、331Vuは第566面、331Vvは第567面、331Vwは第568面、331Vxは第569面、331Vyは第570面、331Vzは第571面、331Waは第572面、331Wbは第573面、331Wcは第574面、331Wdは第575面、331Weは第576面、331Wfは第577面、331Wgは第578面、331Whは第579面、331Wiは第580面、331Wjは第581面、331Wkは第582面、331Wlは第583面、331Wmは第584面、331Wnは第585面、331Woは第586面、331Wpは第587面、331Wqは第588面、331Wrは第589面、331Wsは第590面、331Wtは第591面、331Wuは第592面、331Wvは第593面、331Wwは第594面、331Wxは第595面、331Wyは第596面、331Wzは第597面、331Xaは第598面、331Xbは第599面、331Xcは第600面、331Xdは第601面、331Xeは第602面、331Xfは第603面、331Xgは第604面、331Xhは第605面、331Xiは第606面、331Xjは第607面、331Xkは第608面、331Xlは第609面、331Xmは第610面、331Xnは第611面、331Xoは第612面、331Xpは第613面、331Xqは第614面、331Xrは第615面、331Xsは第616面、331Xtは第617面、331Xuは第618面、331Xvは第619面、331Xwは第620面、331Xxは第621面、331Xyは第622面、331Xzは第623面、331Yaは第624面、331Ybは第625面、331Ycは第626面、331Ydは第627面、331Yeは第628面、331Yfは第629面、331Ygは第630面、331Yhは第631面、331Yiは第632面、331Yjは第633面、331Ykは第634面、331Ylは第635面、331Ymは第636面、331Ynは第637面、331Yoは第638面、331Ypは第639面、331Yqは第640面、331Yrは第641面、331Ysは第642面、331Ytは第643面、331Yuは第644面、331Yvは第645面、331Ywは第646面、331Yxは第647面、331Yyは第648面、331Yzは第649面、331Zaは第650面、331Zbは第651面、331Zcは第652面、331Zdは第653面、331Zeは第654面、331Zfは第655面、331Zgは第656面、331Zhは第657面、331Ziは第658面、331Zjは第659面、331Zkは第660面、331Zlは第661面、331Zmは第662面、331Znは第663面、331Zoは第664面、331Zpは第665面、331Zqは第666面、331Zrは第667面、331Zsは第668面、331Ztは第669面、331Zuは第670面、331Zvは第671面、331Zwは第672面、331Zxは第673面、331Zyは第674面、331Zzは第675面、331Aaは第676面、331Abは第677面、331Acは第678面、331Adは第679面、331Aeは第680面、331Afは第681面、331Agは第682面、331Ahは第683面、331Aiは第684面、331Ajは第685面、331Akは第686面、331Alは第687面、331Amは第688面、331Anは第689面、331Aoは第690面、331Apは第691面、331Aqは第692面、331Arは第693面、331Asは第694面、331Atは第695面、331Auは第696面、331Avは第697面、331Awは第698面、331Axは第699面、331Ayは第700面、331Azは第701面、331Baは第702面、331Bbは第703面、331Bcは第704面、331Bdは第705面、331Beは第706面、331Bfは第707面、331Bgは第708面、331Bhは第709面、331Biは第710面、331Bjは第711面、331Bkは第712面、331Blは第713面、331Bmは第714面、331Bnは第715面、331Boは第716面、331Bpは第717面、331Bqは第718面、331Brは第719面、331Bsは第720面、331Btは第721面、331Buは第722面、331Bvは第723面、331Bwは第724面、331Bxは第725面、331Byは第726面、331Bzは第727面、331Caは第728面、331Cbは第729面、331Ccは第730面、331Cdは第731面、331Ceは第732面、331Cfは第733面、331Cgは第734面、331Chは第735面、331Ciは第736面、331Cjは第737面、331Ckは第738面、331Clは第739面、331Cmは第740面、331Cnは第741面、331Coは第742面、331Cpは第743面、331Cqは第744面、331Crは第745面、331Csは第746面、331Ctは第747面、331Cuは第748面、331Cvは第749面、331Cwは第750面、331Cxは第751面、331Cyは第752面、331Czは第753面、331Daは第754面、331Dbは第755面、331Dcは第756面、331Ddは第757面、331Deは第758面、331Dfは第759面、331Dgは第760面、331Dhは第761面、331Diは第762面、331Djは第763面、331Dkは第764面、331Dlは第765面、331Dmは第766面、331Dnは第767面、331Doは第768面、331Dpは第769面、331Dqは第770面、331Drは第771面、331Dsは第772面、331Dtは第773面、331Duは第774面、331Dvは第775面、331Dwは第776面、331Dxは第777面、331Dyは第778面、331Dzは第779面、331Eaは第780面、331Ebは第781面、331Ecは第782面、331Edは第783面、331Eeは第784面、331Efは第785面、331Egは第786面、331Ehは第787面、331Eiは第788面、331Ejは第789面、331Ekは第790面、331Elは第791面、331Emは第792面、331Enは第793面、331Eoは第794面、331Epは第795面、331Eqは第796面、331Erは第797面、331Esは第798面、331Etは第799面、331Euは第800面、331Evは第801面、331Ewは第802面、331Exは第803面、331Eyは第804面、331Ezは第805面、331Faは第806面、331Fbは第807面、331Fcは第808面、331Fdは第809面、331Feは第810面、331Ffは第811面、331Fgは第812面、331Fhは第813面、331Fiは第814面、331Fjは第815面、331Fkは第816面、331Flは第817面、331Fmは第818面、331Fnは第819面、331Foは第820面、331Fpは第821面、331Fqは第822面、331Frは第823面、331Fsは第824面、331Ftは第825面、331Fuは第826面、331Fvは第827面、331Fwは第828面、331Fxは第829面、331Fyは第830面、331Fzは第831面、331Gaは第832面、331Gbは第833面、331Gcは第834面、331Gdは第835面、331Geは第836面、331Gfは第837面、331Ggは第838面、331Ghは第839面、331Giは第840面、331Gjは第841面、331Gkは第842面、331Glは第843面、331Gmは第844面、331Gnは第845面、331Goは第846面、331Gpは第847面、331Gqは第848面、331Grは第849面、331Gsは第850面、331Gtは第851面、331Guは第852面、331Gvは第853面、331Gwは第854面、331Gxは第855面、331Gyは第856面、331Gzは第857面、331Haは第858面、331Hbは第859面、331Hcは第860面、331Hdは第861面、331Heは第862面、331Hfは第863面、331Hgは第864面、331Hhは第865面、331Hiは第866面、331Hjは第867面、331Hkは第868面、331Hlは第869面、331Hmは第870面、331Hnは第871面、331Hoは第872面、331Hpは第873面、331Hqは第874面、331Hrは第875面、331Hsは第876面、331Htは第877面、331Huは第878面、331Hvは第879面、331Hwは第880面、331Hxは第881面、331Hyは第882面、331Hzは第883面、331Iaは第884面、331Ibは第885面、331Icは第886面、331Idは第887面、331Ieは第888面、331Ifは第889面、331Igは第890面、331Ihは第891面、331Iiは第892面、331Ijは第893面、331Ikは第894面、331Ilは第895面、331Imは第896面、331Inは第897面、331Ioは第898面、331Ipは第899面、331Iqは第900面、331Irは第901面、331Isは第902面、331Itは第903面、331Iuは第904面、331Ivは第905面、331Iwは第906面、331Ixは第907面、331Iyは第908面、331Izは第909面、331Jaは第910面、331Jbは第911面、331Jcは第912面、331Jdは第913面、331Jeは第914面、331Jfは第915面、331Jgは第916面、331Jhは第917面、331Jiは第918面、331Jjは第919面、331Jkは第920面、331Jlは第921面、331Jmは第922面、331Jnは第923面、331Joは第924面、331Jpは第925面、331Jqは第926面、331Jrは第927面、331Jsは第928面、331Jtは第929面、331Juは第930面、331Jvは第931面、331Jwは第932面、331Jxは第933面、331Jyは第934面、331Jzは第935面、331Kaは第936面、331Kbは第937面、331Kcは第938面、331Kdは第939面、331Keは第940面、331Kfは第941面、331Kgは第942面、331Khは第943面、331Kiは第944面、331Kjは第945面、331Kkは第946面、331Klは第947面、331Kmは第948面、331Knは第949面、331Koは第950面、331Kpは第951面、331Kqは第952面、331Krは第953面、331Ksは第954面、331Ktは第955面、331Kuは第956面、331Kvは第957面、331Kwは第958面、331Kxは第959面、331Kyは第960面、331Kzは第961面、331Laは第962面、331Lbは第963面、331Lcは第964面、331Ldは第965面、331Leは第966面、331Lfは第967面、331Lgは第968面、331Lhは第969面、331Liは第970面、331Ljは第971面、331Lkは第972面、331Llは第973面、331Lmは第974面、331Lnは第975面、331Loは第976面、331Lpは第977面、331Lqは第978面、331Lrは第979面、331Lsは第980面、331Ltは第981面、331Luは第982面、331Lvは第983面、331Lwは第984面、331Lxは第985面、331Lyは第986面、331Lzは第987面、331Maは第988面、331Mbは第989面、331Mcは第990面、331Mdは第991面、331Meは第992面、331Mfは第993面、331Mgは第994面、331Mh

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190
 260
 270
 350
 470
 1110
 1120A, 1120B
 1130
 1140
 1150
 1160
 1170
 1180
 1320B, 1320C, 1320D
 1321B, 1321C, 1321D
 1331B, 1331C, 1331D
 1331A, 2

ードフレーム面
 1331Ab
 イニング面
 1410
 ードフレーム面
 1420
 オトレジスト
 1430
 ジストパターン
 1440
 ンナーリード
 1510
 ードフレーム
 1511
 イパッド
 1512
 ンナーリード
 1512A
 ンナーリード先面
 1513
 ワターリード
 1514
 ムバー
 1515
 レーム面 (内面)
 1520
 面表示
 1521
 面 (パッド)
 1530
 1540
 止面

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SECRET - EYES

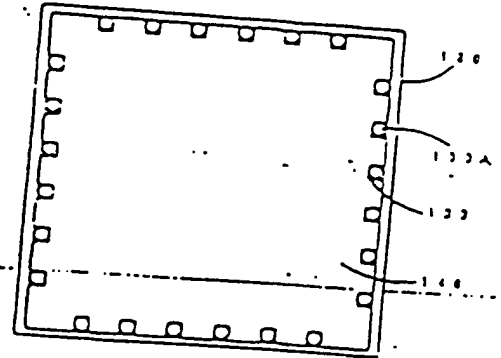
(۱)



(c)



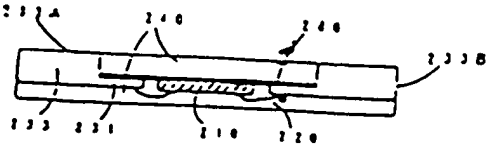
(d)



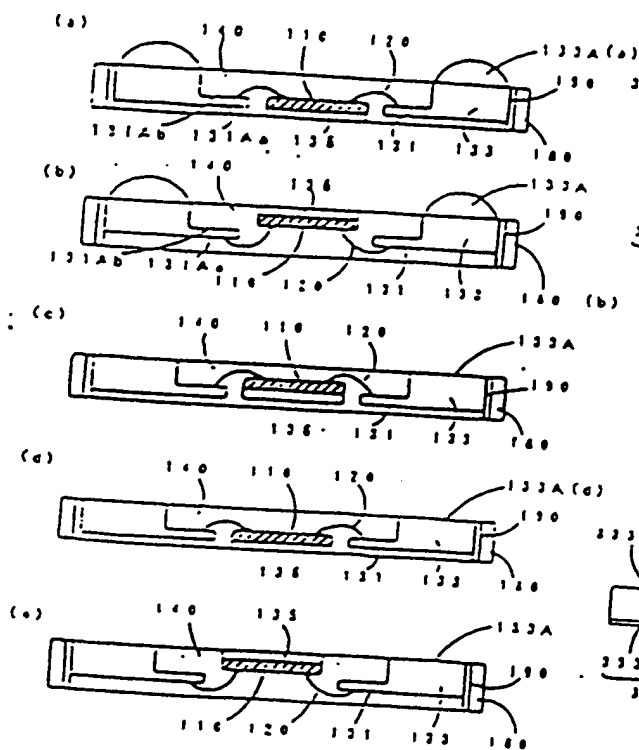
(۱)



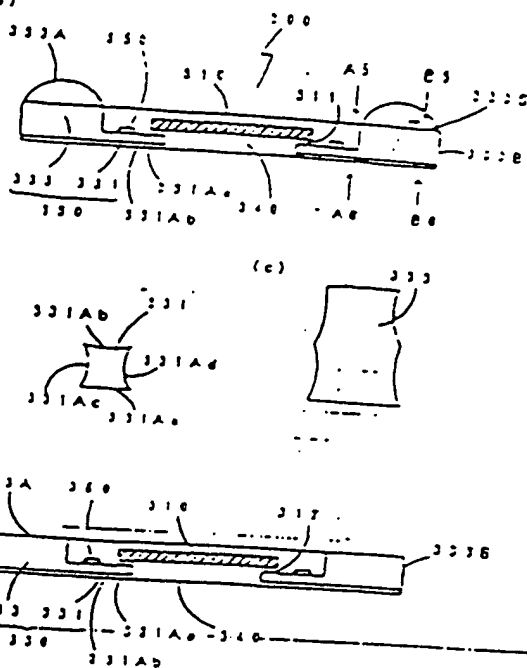
(c)



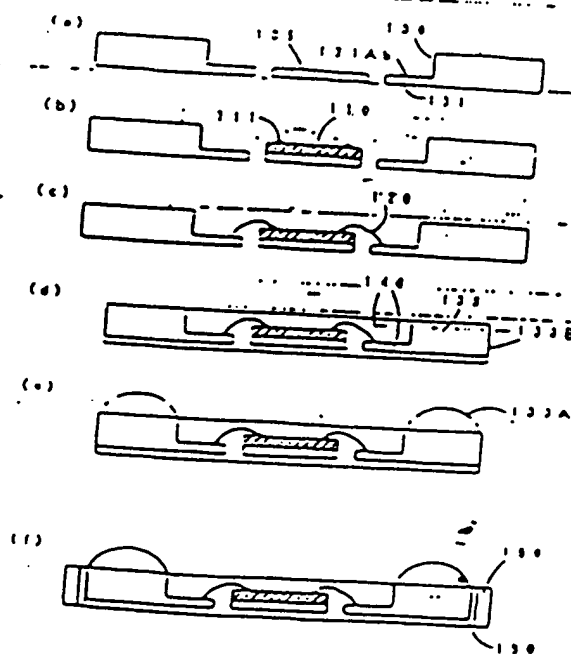
(३३)



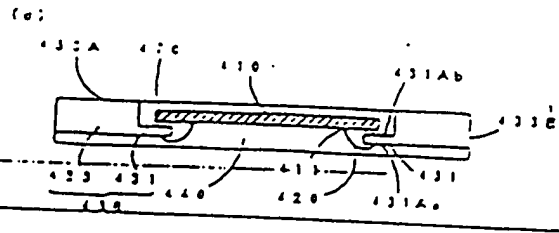
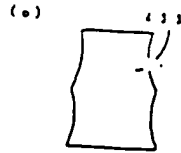
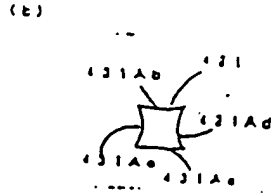
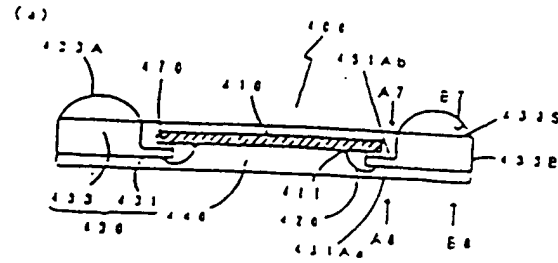
(5 6)



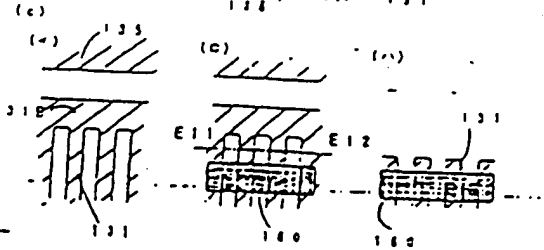
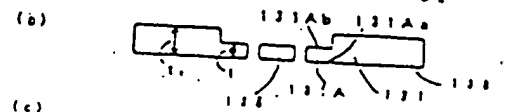
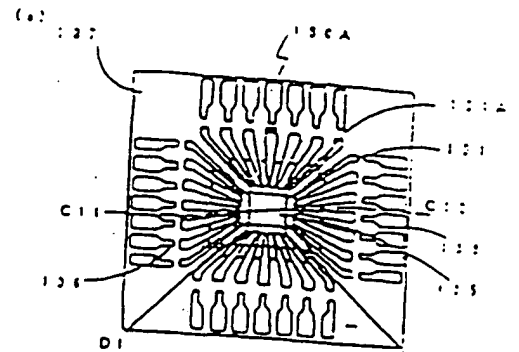
(2 9)



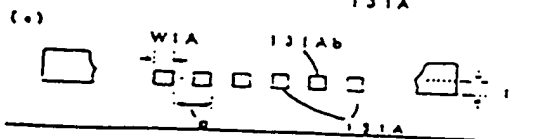
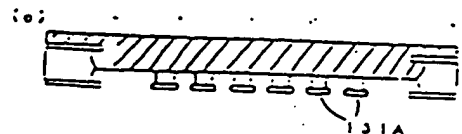
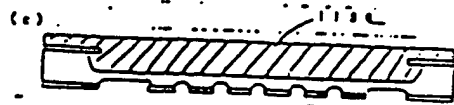
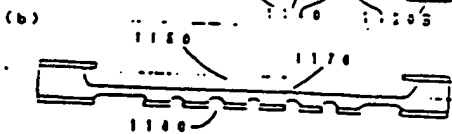
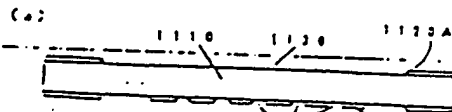
(27)



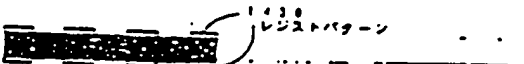
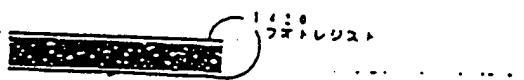
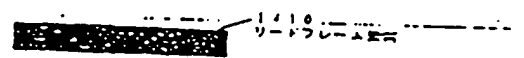
(55)



(211)



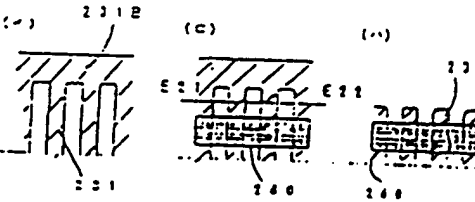
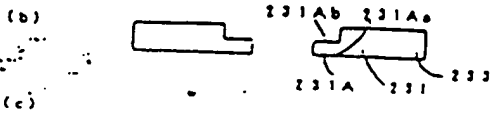
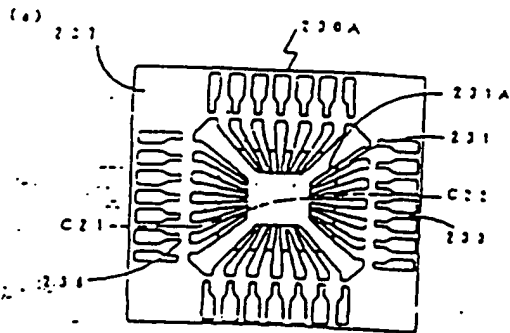
(214)



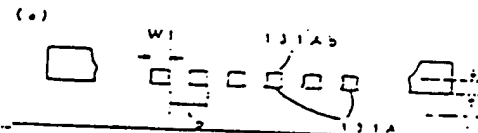
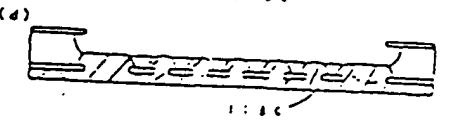
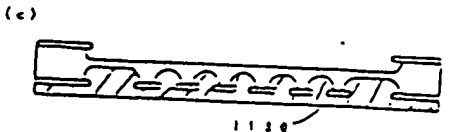
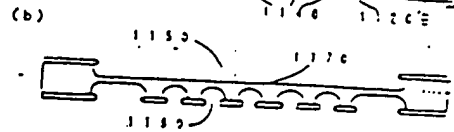
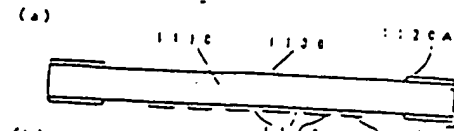
(14)

FIG 9-6205

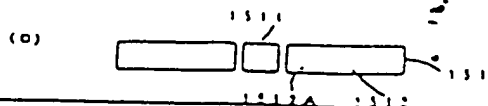
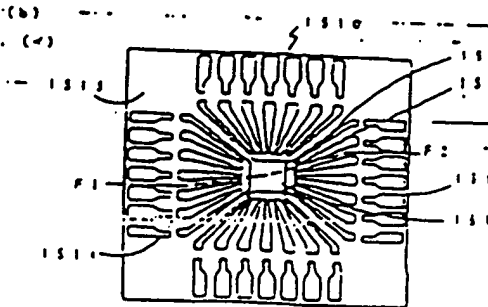
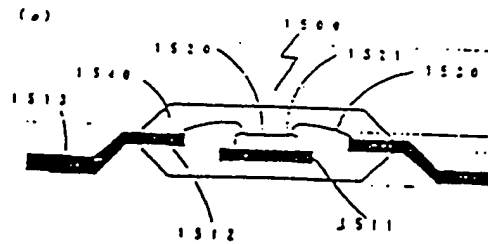
(210)



(212)



(215)



(4)

